



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,026	08/14/2000	Paul A. Farrar	M4065.0082/P082-A	8833

24998 7590 11/05/2002

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER

PAREKH, NITIN

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 11/05/2002

9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

09/638,026

FARRAR, PAUL A. *gh*

Examiner

Art Unit

Nitin Parekh

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 40,43-51 and 68-72 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 40,43-51 and 68-72 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 40, 43-51, 68-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) in view of Akram (US Pat. 5808360), the admitted prior art (APA) and Gochnour et al (US Pat. 5678301).

Regarding claim 40, Yamamoto discloses a semiconductor device comprising:

- a semiconductor structure having a metal contact (23 in Fig. 7) formed on the surface thereof
- a first insulator layer (24/41 in Fig. 7) overlying the metal contact
- a metal pad/interconnection (50 in Fig. 7) overlying the first insulator layer and in contact with the metal contact, the metal pad being partially overtop of the metal contact
- a second insulator layer (47 in Fig. 7) overlying the metal pad

Art Unit: 2811

- the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) in the first insulator, and
- solder contact/ball (48 in Fig. 7) formed in the second insulator layer and in contact with the metal pad, the solder contact/ball extending from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (Fig. 7)

(Fig. 7; Col. 6, line 40- Col. 7, line 5; Col. 4-8).

Yamamoto fails to specify the diameter of the solder contact/ball being less than 15, 10, 2 microns or between 2-15 microns.

The APA discloses using conventional 100 microns diameter solder balls in C4 bonding of an integrated circuit/wafer to a substrate such as module or circuit board.

Akram teaches using solder microbumps having a diameter ranging from 15-100 microns (30 in Fig. 1C; Col. 5, line 7- 32) in a flip chip interconnection. Akram further teaches using the microbumps having mushroom/hemispherical shaped top/tip portion where the total height (Fig. 1C and 3) is in the range of 1-60 microns and the diameter of the microbumps being smaller than the pad dimension (Col. 5, line 1-16). The Fig. 1C and 3 of Akram show the dimensions and the relative comparison of the total height and diameter of the microbumps and pad dimension. It would be obvious to one of ordinary skill in the art to realize that the microbumps can have the diameter in a range of 1-60 microns.

Art Unit: 2811

Akram further teaches the conventional devices of the prior art where such microbumps/contacts are formed on a die and the die being mounted on a substrate (Col. 1, line 30-50).

Gochmour et al teach using solder contacts/microbumps having a diameter between 8-50 microns on a substrate where the substrate in a form of a wafer which is conventionally diced into chips/dice (Fig. 3A and 7; Col. 3, line 50- Col. 4, line 26).

Furthermore, the selection of parameters such as size/dimension, a range and shape of the solder contacts including diameter, pitch/spacing, pad dimension, thickness of an insulating layer, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired I/O density, performance and reliability.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the solder contacts having diameter less than 15, 10, 2 microns or between 2-15 microns so that I/O connection density and performance can be improved and the device size can be reduced using Akram, APA and Gochmour et al's microbump configurations in Yamamoto's device.

Regarding claims 43-51, 71 and 72, the claim elements have been addressed in the rejection as explained above for claim 1.

Art Unit: 2811

Regarding claim 68, Yamamoto discloses the first insulating layer being 10-50 microns thick (Col. 4, line 39) but fails to specify the first insulating layer being 2 microns thicker than the metal contact. However, it can be clearly seen in Fig. 7 of Yamamoto's device that the first insulating layer (41/24 in Fig. 7; Col. 4, line 39)) is 2-3 times thicker than the metal pad which is conventionally approximately 10 microns thick (see Akram, Col. 4, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first insulating layer being 2 microns thicker than the metal contact so that the reliability of the passivation/insulation of the interconnect can be improved in Yamamoto's device in view of Akram, APA and Gochnour et al.

Regarding claims 69 and 70, Yamamoto further discloses the metal pad/interconnection comprising a stack of four different metals comprising Zinc, Nickel, Copper, Gold (43/44/45/46A/46B/50 in Fig. 7; Col. 5, line 9-35) but fails to specify using Zirconium as one of the four metals. It is conventional in the chip packaging and interconnection technology art to use metals such as Nickel, Copper, Gold, Zirconium, Palladium, etc. in forming metal pad/interconnection.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal pad comprising a stack of four different metal levels comprising Zirconium, Nickel, Copper and Gold so that the

Art Unit: 2811

electrical parameters/properties of the interconnect can be improved in Yamamoto's device in view of Akram, APA and Gochnour et al.

Response to Arguments

4. Applicant's arguments with respect to claims 40, 43-51 and 68-72 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

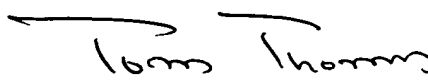
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP

November 1, 2002


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800